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December 28, 2001 — Date

Denise Sheridan

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Brian W. Huber and David R. Brown	Attorney Docket No.:	500125.02
Serial No.	: 10/007,871	Group Art Unit	: Not yet assigned
Filed	: November 13, 2001	Examiner	: Not yet assigned
Title	: METHOD AND APPARATUS FOR PHASE-SPLITTING A CLOCK SIGNAL		

SUPPLEMENTAL PRELIMINARY AMENDMENT

Box Non-Fee Amendment
Commissioner of Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified application as follows:

In the Title:

Please replace the title with the following rewritten title:

-- METHOD OF SCALING DIGITAL CIRCUITS AND CONTROLLING THE TIMING RELATIONSHIP BETWEEN DIGITAL CIRCUITS --

In the Specification:

Please replace the paragraph beginning at page 9, line 23, with the following rewritten paragraph:

-- In the field of semiconductors, it is common to scale up or down the size of components in circuits depending upon the load to be driven by the circuit. Thus, the inverters used in the phase splitters 40, 40', 80, 80', 100, 102. However, as also understood in the art, there is a limit to how small semiconductor components can be scaled. Thus, when the phase splitters 40, 40', 80, 80', 100, 102 are scaled to their minimum size, the relative size of the inverters can change. In particular, the output inverters 48, 54 can continue to be scaled downwardly beyond the point that the input inverters 46, 50 can no longer be scaled down.

When scaling semiconductor circuits in this manner, it is desirable for the timing relationships in the circuit to be insensitive to the scaling. However, when the ratio of the scaling of the output inverters 48, 54 to the scaling of the input inverters 46, 50 changes because the input inverters 46, 50 have reached their minimum sizes, the timing relationships in the phase splitter change. The timing relationship changes because the input inverters 46, 50 have been made larger relative to the size of the output inverters 48, 52, and are thus more easily able to drive the output inverters 48, 52. The signal from the output inverters 48, 52 thus transitions earlier relative to 2the transition of a clock signal applied to the input of the input inverters 46, 50. As a result, the scaling of the phase splitter alters the timing of the phase splitter. --

In the Claims:

Please amend claims 88 and 89, and add new claims 90-97 as follows:

88. (Amended) A method of scaling a circuit having at least a first logic component driving a second logic component, the method comprising:

downwardly scaling the first logic component;

downwardly scaling the second logic component to a greater extent than the scaling of the first logic component so that the second logic component is scaled to a greater extent than the first logic component; and

coupling an electrical loading component to the output of the first logic component, the electrical component being unconnected to any other portion of the circuit, the electrical loading component maintaining a timing relationship between the first and second logic components.

89. (Amended) The method of claim 88, wherein each of the first and second logic components comprises respective inverters, and wherein the electrical component comprises an inverter.

--90. A method of scaling a circuit having at least a first logic component driving a second logic component, the method comprising:

downwardly scaling the first and second logic components, one of the logic components being scaled to a lesser extent than the other of the logic components; and

coupling an electrical loading component to the output of the logic component that is scaled to the lesser extent, the electrical component being unconnected to any other circuitry that is coupled to the first and second logic components.

91. The method of claim 90 wherein a characteristic of the electrical loading component is selected to maintain a timing relationship between the first and second logic components.

92. The method of claim 90 wherein the act of downwardly scaling the first and second logic components comprises downwardly scaling the first logic component to a lesser extent than the downward scaling of the second logic component.

93. The method of claim 90 wherein the act of coupling an electrical loading component to the output of the logic component that is scaled to the lesser extent comprises coupling an input terminal of an inverter to the output of the logic component that is scaled to the lesser extent, the inverter having an output terminal that is left unconnected to any other portion of the circuitry that is coupled to the first and second logic components.

94. A method of controlling the timing relationship between first and second logic components, the method comprising coupling an electrical loading component to the output of one of the logic components, the electrical component being unconnected to any other circuitry.

95. The method of claim 94 wherein the first logic component drives the second logic component.

96. The method of claim 95, wherein the act of coupling an electrical loading component to the output of one of the logic components comprises coupling an electrical loading component to the output of the first logic component.

97. The method of claim 90 wherein the act of coupling an electrical loading component to the output of one of the logic components comprises coupling an input terminal of an inverter to an output of one of the logic components, the inverter having an output terminal that is left unconnected to any other circuitry.--

REMARKS

The title is being amended to more accurately describe the claimed subject matter, and the specification is being amended to correct informalities noted by applicant's attorneys.

The changes to the drawings are being made to include Figures 6 and 7 as described in the specification. New Figure 8 is the same as prior Figure 6, and is described in the specification as Figure 8. New Figures 9 and 10 are identical to prior Figures 7 and 8, and are described in the specification as Figures 9 and 10, respectively. No new matter is being added since new Figures 6 and 7 are exactly as described in the specification as filed.

Finally, the claims are being amended to place them in better form, and new claims are being added.

Respectfully submitted,

DORSEY & WHITNEY LLP

Kimton N. Eng
Registration No. 43,605

KNE (EWB):dms
Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)
Request for Drawing Change (Figs. 6-10)
Formal Drawings (4 Sheets, Figs. 1-10)
Information Disclosure Statement
Form PTO-1449

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

The title has been amended as follows:

[METHOD AND APPARATUS FOR PHASE-SPLITTING A CLOCK SIGNAL] METHOD OF SCALING DIGITAL CIRCUITS AND CONTROLLING THE TIMING RELATIONSHIP BETWEEN DIGITAL CIRCUITS

In the Specification:

Paragraph beginning at line 23 of page 9 has been amended as follows:

In the field of semiconductors, it is common to scale up or down the size of components in circuits depending upon the load to be driven by the circuit. Thus, the inverters used in the phase splitters 40, 40', 80, 80', 100, 102. However, as also understood in the art, there is a limit to how small semiconductor components can be scaled. Thus, when the phase splitters 40, 40', 80, 80', 100, 102 are scaled to their minimum size, the relative size of the inverters can change. In particular, the output inverters 48, 54 can continue to be scaled downwardly beyond the point that the input inverters 46, 50 can no longer be scaled down. When scaling semiconductor circuits in this manner, it is desirable for the timing relationships in the circuit to be insensitive to the scaling. However, when the ratio of the scaling of the output inverters 48, 54 to the scaling of the input inverters 46, 50 changes because the input inverters 46, 50 have reached their minimum sizes, the timing relationships in the phase splitter change. The timing relationship changes because the input inverters 46, 50 have been made larger relative to the size of the output inverters 48, [54]52, and are thus more easily able to drive the output inverters [46, 50]48, 52. The signal from the output inverters [46, 50]48, 52 thus transitions earlier relative to the transition of a clock signal applied to the input of the input inverters 46, 50. As a result, the scaling of the phase splitter alters the timing of the phase splitter.

In the Claims:

Claims 88-89 have been amended and new claims 90-97 added as follows:

downwardly scaling the first logic component;

downwardly scaling the second logic component to a greater extent than the scaling of the first logic component so that the second logic component is scaled to a greater extent than the first logic component; and

coupling an electrical loading component to the output of the first logic component, the electrical component being unconnected to any other portion of the circuit, the electrical loading component [maintining]maintaining [the]a timing [relat]relationship between the first and second logic components.

89. (Amended) The method of claim 88, wherein each of the first and second logic components comprises [a]respective inverters, and wherein [each of]the electrical component[s] comprises [a respective]an inverter.

--90. A method of scaling a circuit having at least a first logic component driving a second logic component, the method comprising:

downwardly scaling the first and second logic components, one of the logic components being scaled to a lesser extent than the other of the logic components; and

coupling an electrical loading component to the output of the logic component that is scaled to the lesser extent, the electrical component being unconnected to any other circuitry that is coupled to the first and second logic components.

91. The method of claim 90 wherein a characteristic of the electrical loading component is selected to maintain a timing relationship between the first and second logic components.

92. The method of claim 90 wherein the act of downwardly scaling the first and second logic components comprises downwardly scaling the first logic component to a lesser extent than the downward scaling of the second logic component.

93. The method of claim 90 wherein the act of coupling an electrical loading component to the output of the logic component that is scaled to the lesser extent comprises

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Title	: METHOD AND APPARATUS FOR PHASE-SPLITTING A CLOCK SIGNAL		

REQUEST FOR DRAWING CHANGE

Box Non-Fee Amendment
Commissioner of Patents
Washington, D.C. 20231

Sir:

Drawing changes, as indicated in red on the attached drawings and as described in the Supplemental Preliminary Amendment Remarks, filed herewith, are hereby submitted for approval by the Examiner.

Respectfully submitted,

DORSEY & WHITNEY LLP

Kimton N. Eng
Registration No. 43,605

Enclosures:
Postcard
Figures 6-10

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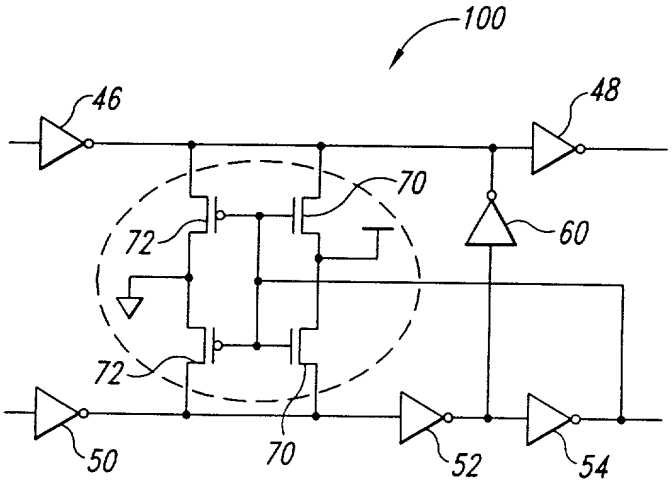
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Fig. 6

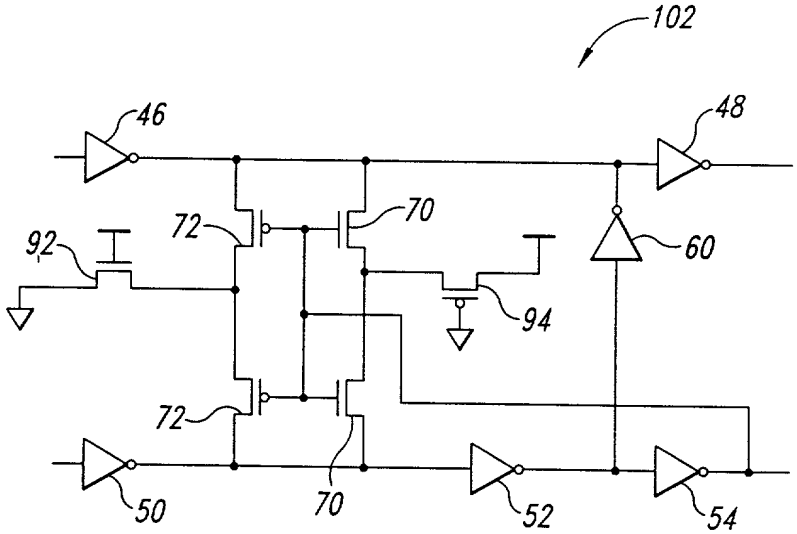
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Fig. 7

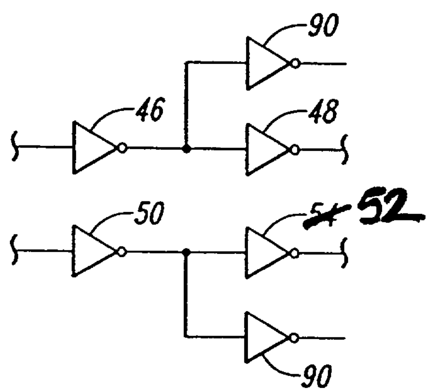

Fig. 8

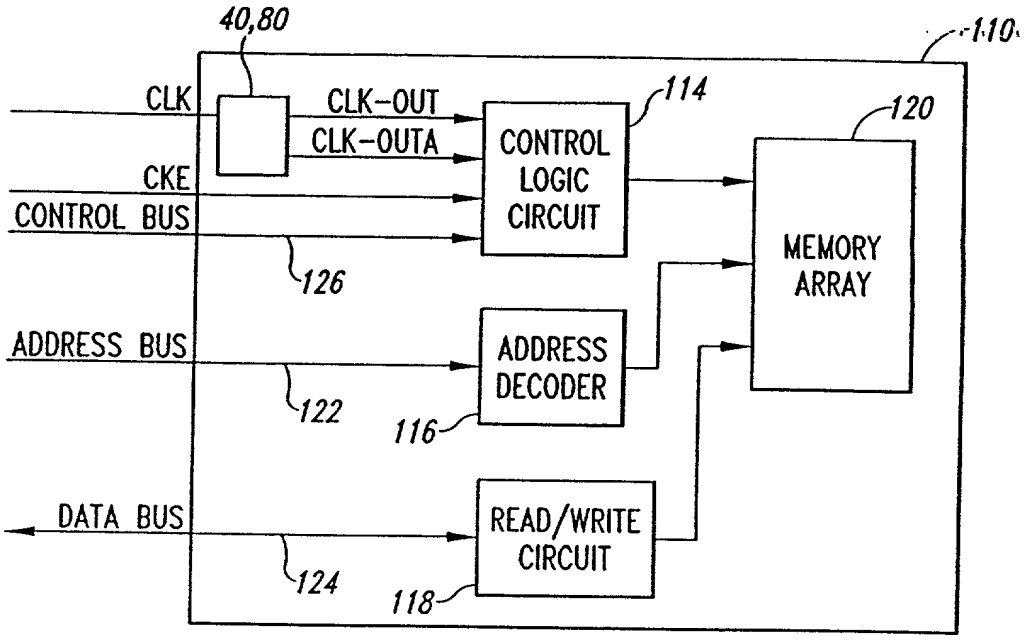

Fig. ~~7~~ 9

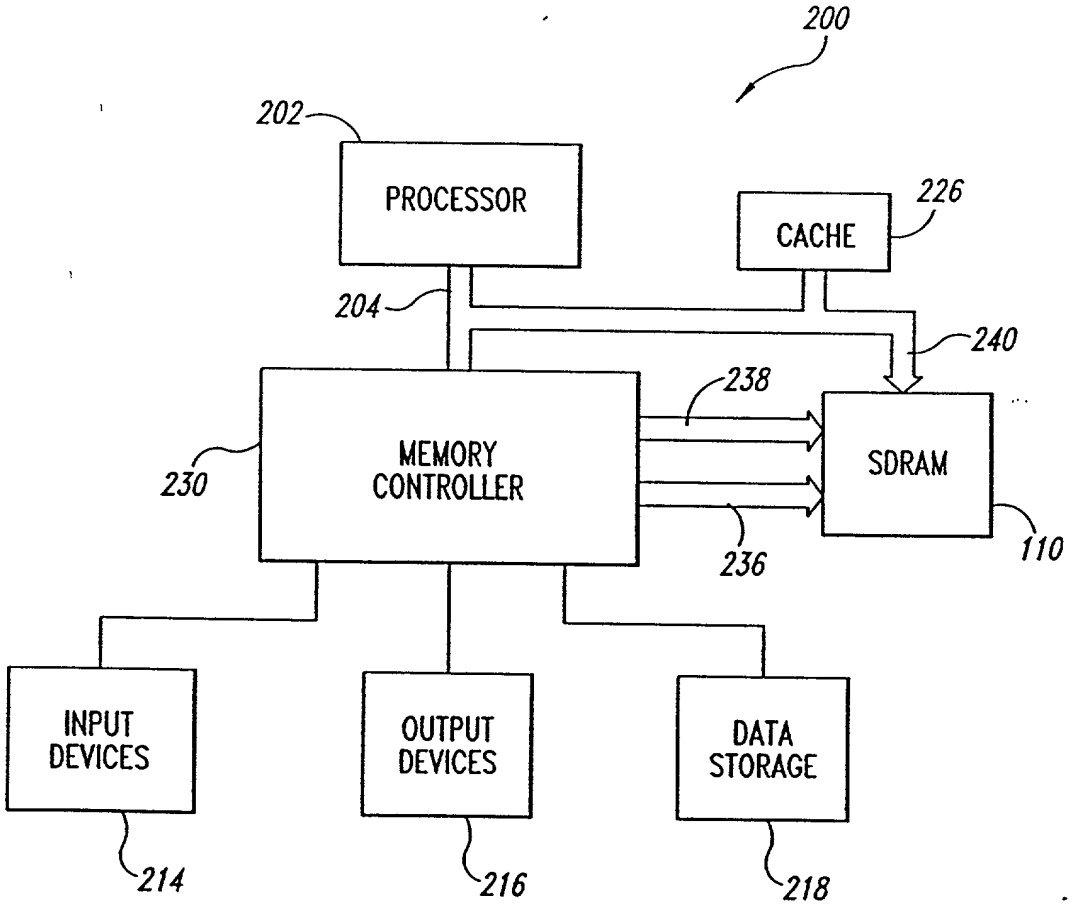

Fig. ~~8~~ 10